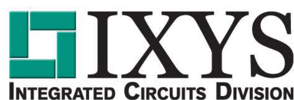

Reliability Report

IXD_602 Series VIS Foundry; Process CU05UMS12010

(ASSEMBLY IN SOIC STYLE PACKAGES)

Report Title: Reliability Summary Report
IXD_602 Series VIS Foundry Process CU05UMS12010
SOIC Style Package Assembly

Report Number: 2011-003

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Introduction:

This report summarizes the Reliability data of IXYS IC Division IXD_602 product family in SOIC style packages. The Reliability data presented here were collected from multiple sources including internal product qualifications, external subcontracted test and reliability facilities and internal reliability monitors. The IXD_602 family of Gate Driver products is foundered at Vanguard International Semiconductor, Corp. (VIS) and assembled at CEI in Thailand and/or Atec in the Philippines. The VIS process is CU05UMS12010.

Reliability Tests:

Table 1 below provides the reliability tests that were performed, the referenced industry specification and details on number of devices/lots per test.

IXD_602SI/SIA Product Reliability Tests

Stress Test	Applicable Specs	Stress Conditions	Number of Lots	Sample Size (SS)	Total SS
HTOL HTOL	JESD22-A104-C Mil-Std-883	1000hrs, 150°C 1000hrs. 125°C	6 2	80 77	480 154
HAST	JESD22-A110-C	130°C, 85% 18.8PSI, 96hrs	6/2	80/76	632
Thermal Shock	Mil-Std-883, M1011	0 to 100°C, 10/10 dwells, 15 cycles	1	55	55
Temp Cycle (T/C)	JESD22-A104-C	-65 to 150°C, 10/10 dwells, 250 cycles	1	55	55
High Temp Storage	JESD22-A103C	150°C, 1000hrs	3	50	150
Autoclave	J-STD-020D.1, JESD22-A102	T=121°C, RH=100% t=96hrs unbiased	6	80	480
Latch Up	AECQ100-003	T=125°C, 35v, 100mA	1	8	8
MSL	J-Std-020	IR reflow; Level 1 3x	1	50	50

Stress Test	Applicable Specs	Stress Conditions	Number of Lots	Sample Size (SS)	Total SS
	Gate Leakage	T=RT	1	8	8
ELFR	AECQ100-008-REV A	T=150°C, t=48hrs With bias	2	800	1600
PTC	JESD22-A105-C	T=-40°C/+125°C, 1000 cycles t=45 min	1	48	48
ESD HBM	JESD22-A114-E	1.5kΩ, 100pF	2/1	9/25	43

Reliability Test Results:

The stress tests and associated results for the reliability analysis of product IXDx602SI/SIA are summarized in Table 2. The devices chosen for the qualification were from standard material manufactured through normal production test flow and electrically tested to datasheet limits prior to stressing. Products selected for the data summary share identical wafer fabrication processes, the same subcontractor assembly locations and all materials related to assembly are identical. Then reliability stresses were conducted and electrically tested to datasheet limits at each interval and final readpoint.

Table 2: Product IXD_602 Family Reliability Test Results

Stress Test	Readpoint / (Reject/ SS)
HTOL 150°C HTOL 125°C	1000 hrs/ 0 / 480 1000 hrs/ 0 / 154
HAST	96 hrs/ 0 /632
Thermal Shock	15 cycles/ 0 /55
Temp Cycle	250 Cycles/ 0 / 55
High Temp Storage	1000 hrs/ 0 / 150
Autoclave	96 hrs / 0 / 480

Stress Test	**Readpoint / (Reject/ SS)**
MSL; IR Reflow 3X	Level 1, 3x/ 0 / 50
Latch-Up	Trigger Pulse
	0/8
Gate Leakage	Neg./Pos. Potential
	0/8
ELFR	48 hrs.
	0/1600
PTC	1000 cycles
	0/48

ESD Testing Results:

As part of this reliability testing, the IXD_602 product family was subjected to Human Body Model (HBM) ESD Sensitivity Classification testing using a KeyTek Zapmaster system. The results are summarized in Table 3. All samples were electrically tested to data sheet limits before and after ESD stressing and they passed after +/-3000V testing.

Table3: Product IXDI602SIA ESD Characterization Results

ESD Model	**Package**	**ESD Test Spec**	**RC Network**	**Highest Passed**	**Class**
HBM	SOIC – 8L	JESD22, A114-E	1.5kΩ, 100pF	3000V	2

FIT (Failure in Time) Rate on the IXD_602 Product Family

Table 4 summarizes the number of devices used for IXD_602 product family reliability stress. Using the HTOL data, FITs were calculated based on the Acceleration Factor (AF) and equivalent device hours at 0.7eV of activation energy for 150°C test temperature and 40°C use temperatures. Using the HAST data, FITs were calculated based on the Acceleration Factor (AF) and equivalent device hours at 0.7eV of activation energy for 130°C test temperature and 40°C use temperatures.

Table 4: Product Family IXD_602SI (SOIC style package data) FIT Rate Summary

(HTOL results were calculated using the higher temperature results at 150 degrees only)

Stress	# of Devices	# of Fails	Hours Tested	Act. Energy	Acceleration Factor	Equivalent Dev. Hours	FIT Rate @ 60% CL
HTOL	480	0	1000	0.7	853.34	409,605,288	2.25
HAST	632	0	96	0.7	1.4318E+03	904,888,485	1.02