

**Industry's First
Optically Coupled
I²C Bus Repeaters**

CPC5903

Optically Coupled I²C Bus Repeater

Providing 3750V_{rms} Galvanic Input-to-Output Isolation

Features:

- Low EM and RF Generation - No Internal Clock
- Bidirectionally Buffers I²C SDA Signal
- Unidirectionally Buffers I²C SCL Signal
- Extends and Isolates I²C Interfaces
- Supports Standard and Fast-mode I²C (400kbps)
- Supports Direct Static-State Buffering Without Refresh
- Operates on 2.7V to 5.5V
- Glitch-Free Operation
- Translates Voltage Levels

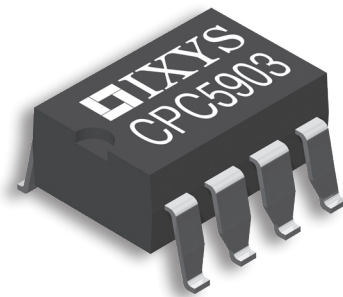
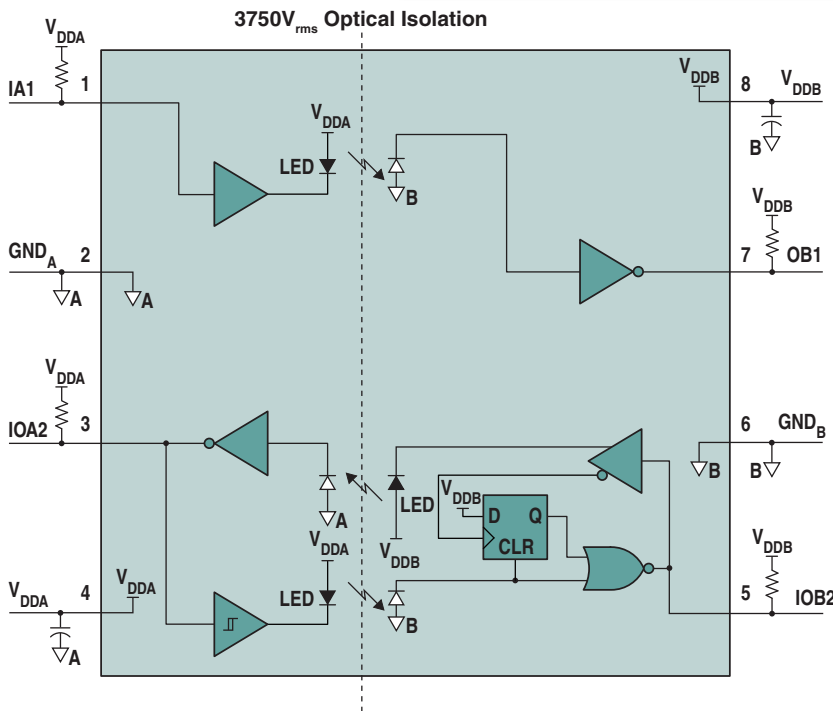
Robust:

- Immune to External EMI and RFI
- High Voltage Isolation - Tested Above 6kV_{pk} for Adverse Environments

Example Applications:

- Power Over Ethernet
- I²C Bus Length Extender
- Isolated Signal Monitoring and Control
- Power Supply High-Side Interface

CPC5903 Functional Block Diagram

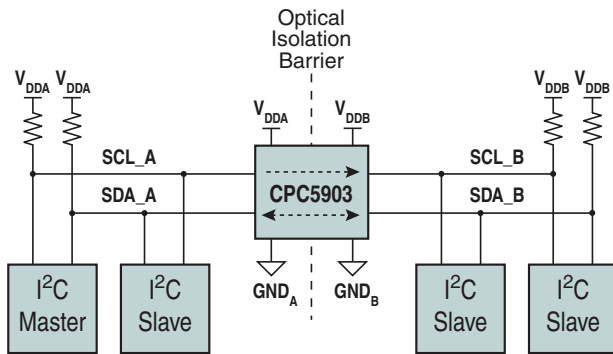


- UL 1577 Certified Component: File E76270
- EN/IEC 60950 Certified Component: TUV Certificate: B 11 10 49410 007

Download IXYS Integrated Circuits Division's Technical Brief, TB-101 "Optically Isolating an I²C Interface:

[http://www.ixysic.com/home/pdfs.nsf/www/TB-101.pdf/\\$file/TB-101.pdf](http://www.ixysic.com/home/pdfs.nsf/www/TB-101.pdf/$file/TB-101.pdf)

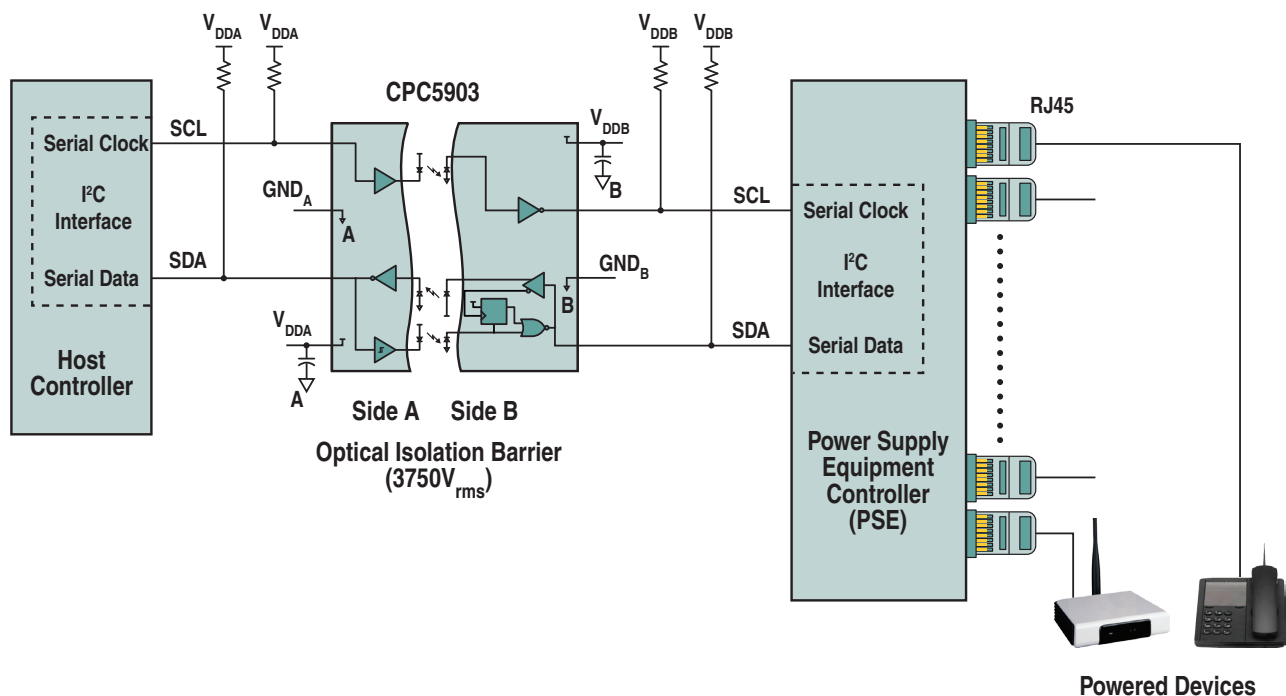
CPC5903 Optically Coupled Bus Repeater: I²C Bus Application



- Replaces Multiple Logic Optoisolators
- 3750V_{rms} Galvanic Isolation
- I²C Fast-mode Operation up to 400kbps
- Bidirectionally Buffers I²C SDA Signal
- Unidirectionally Buffers I²C SCL Signal
- Internal Glitch Suppression Circuitry
- Supports Bus Level Translation: 2.7V to 5.5V
- Passes DC Signals - No Refresh Needed

CPC5903 Optically Coupled Bus Repeater: Power-over-Ethernet (PoE) Application

- Provides Communications Interface Between Host Controller and PSE Controller
- Provides 3750V_{rms} Galvanic Isolation Between Host Controller and PSE Controller
- Protects Host Controller During Power Supply Surge Tests
- Bidirectionally Buffers Data Signals Between Host Controller and PSE Controller
- Unidirectionally Buffers Clock Signals From Host Controller to PSE Controller
- Simplifies Bus Design by Replacing Multiple Logic Optoisolators
- Provides any Necessary Bus Level Translation Between Host Controller and PSE Controller



For more information about IXYS Integrated Circuits Division's CPC5903, please visit:
<http://www.ixysic.com/Products/OptBusRepUniBi.htm>

For additional information, contact your IXYS IC Division Representative:
<http://www.ixysic.com/home/pages.nsf/locate.rep>
 Or visit IXYS IC Division's web site:
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